

Notice of References Cited	Application/Control No. 10/008,270	Applicant(s)/Patent Under Reexamination CAVANAGH ET AL.	
	Examiner Jason Proctor	Art Unit 2123	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,881,267	03-1999	Dearth et al.	703/27
*	B	US-5,910,903	06-1999	Feinberg et al.	703/6
	C	US-			
	D	US-			
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	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Dr. Daniel C. Hyde, "CSCI 320 Computer Architecture Handbook on Verilog HDL", copyright 1995, updated August 1997, pages 1-26
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.